

School of Materials Seminar

High-k/Metal Gate Technology for Si CMOS Applications: A Materials Scientists Perspective

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Continued miniaturization of the different physical elements of a Si Metal Oxide Semiconductor Field Effect Transistor (MOSFET) required in order to attain higher chip speeds and greater economies of scale have spurred the need for significant materials innovations. One of the key elements to facilitate scaling has been the silicon oxynitride based gate dielectric of a MOSFET. While traditionally with each technology generation, transistor scaling has been facilitated by simply reducing the thickness of the gate dielectric, the current aggressively scaled thickness ~ 1.2 nm of the gate dielectric ensures that any more thinning of the dielectric would significantly degrade the leakage and performance of the MOSFET. Replacement of the silicon oxynitride dielectric (having a dielectric constant (k) = 3.9), by a physically thicker higher dielectric constant material would enable an electrically thinner equivalent oxide thickness (EOT) while preserving the leakage properties of the MOSFET and thereby enable gate length scaling. The search for a suitable “high-k” dielectric has been an area of intense research within the last decade, with the Si technology industry settling on hafnium-based dielectrics as the high-k dielectric of choice. In this presentation I will discuss some of the key materials issues that delayed the introduction of hafnium based high-k dielectrics including reduced carrier mobility in the channel, oxygen based instabilities such as catalytic SiO_x regrowth and vacancy generation within the Hf based dielectric, and the absence of thermally stable dual metal electrodes. It will be shown that through a combination of materials innovations and engineering ingenuity these issues were successfully overcome, thereby paving the way for high-k/metal gate implementation.

Dr. Narayanan received his B.Tech. in Metallurgical Engineering from the Indian Institute of Technology, Madras (1995), and his M.S. (1996) and Ph.D. (1999) in Materials Science and Engineering from Carnegie Mellon University where his dissertation concentrated on understanding the origins of line and planar defects during the epitaxial growth of Gallium Phosphide on different orientations of Si. In 1999, Dr. Narayanan joined the Department of Chemical and Materials Engineering at Arizona State University as a Post Doctoral Research Associate where his research focus was on the initial stages of nucleation and growth of III-V nitrides on Sapphire and Si substrates grown by MOCVD. Dr. Narayanan joined IBM in 2001. His research at IBM over the past seven years has focused on advanced gate stack technologies including High κ -Metal Gate Processes and Devices. He was awarded an IBM Research Division Award for contributions to High-k/Metal Gates in 2006 and was recognized as an IBM Master Inventor in 2007. Currently, Dr. Narayanan is the Manager of High κ -Metal Gate Process Development for the 22 nm node and beyond within the Silicon Technology Department at the IBM Thomas J. Watson Research Center. He is an author or co-author of over 30 peer-reviewed journal and conference papers and holds 19 patents.

